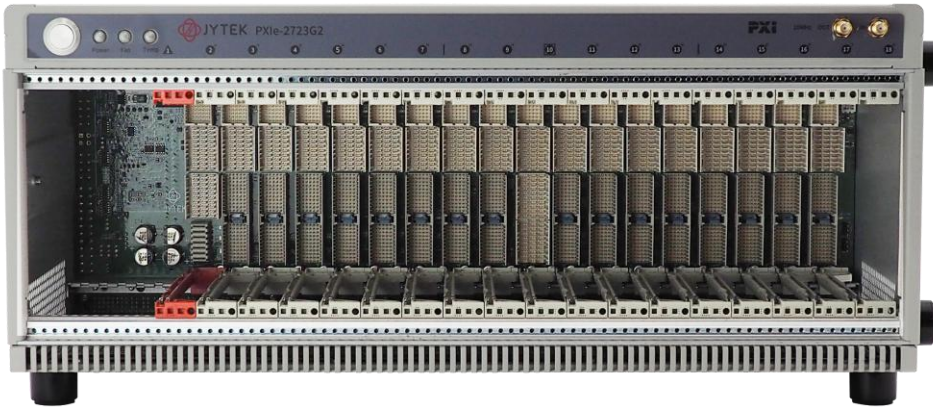
PXIe-2723 Chassis

User Manual



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1. Introduction

1.1 Overview

PXIe-2723 series are flexibility and high performance 18-slot all-hybrid PXIe chassis which features up to 24 GB/s system bandwidth and 58 W of power and cooling in every slot.

Depanding on PCIe link speed capability, PXIe-2723 series provide two models as shown inTable 1.

Model Name	PCIe Link Speed Capability	System Bandwidth	Slot Bandwidth
PXIe-2723G3	Gen3	24 GB/s	8 GB/s
PXIe-2723G2	Gen2	8 GB/s	4 GB/s

Table 1 PXIe-2723 series model name

Note:

- system bandwidth defined as data rate between controller and chassis backplane.
- slot bandwidth defined as data rate between peripheral module and chassis backplane.

1.2 Main Features

- PXI-5 PXI Express hardware specification Rev.1.0 compliant
- High data throughput 18-slot PCIe Gen2 (PXIe-2723G2) or Gen3 (PXIe-2723G3) PXIe chassis
- Up to 24 GB/s (PCI Express 3.0 x8 and x16 link) system bandwidth (PXIe-2723G3)
- Up to 8 GB/s (PCI Express 3.0 x8 link) bandwidth for all peripheral slots (PXIe-2723G3)
- High clock accuracy and low phase jitter
- Low power ripple-noise
- Specially designed for cost effective PXI/PXIe applications
- 0°C to 55°C extended operating temperature range
- Ideal for OEM vendors

2. Hardware

2.1 Backplane Overview

2.1.1 PXIe-2723G3 Backplane Architecture

All of the PXIe peripheral slots can support PCIe Gen3 x8 link providing a maximum slot bandwidth of 8 GB/s. The system slot can support PCIe Gen3 x24 link (x8 + x16) and has a maximum system bandwidth of 24 GB/s.

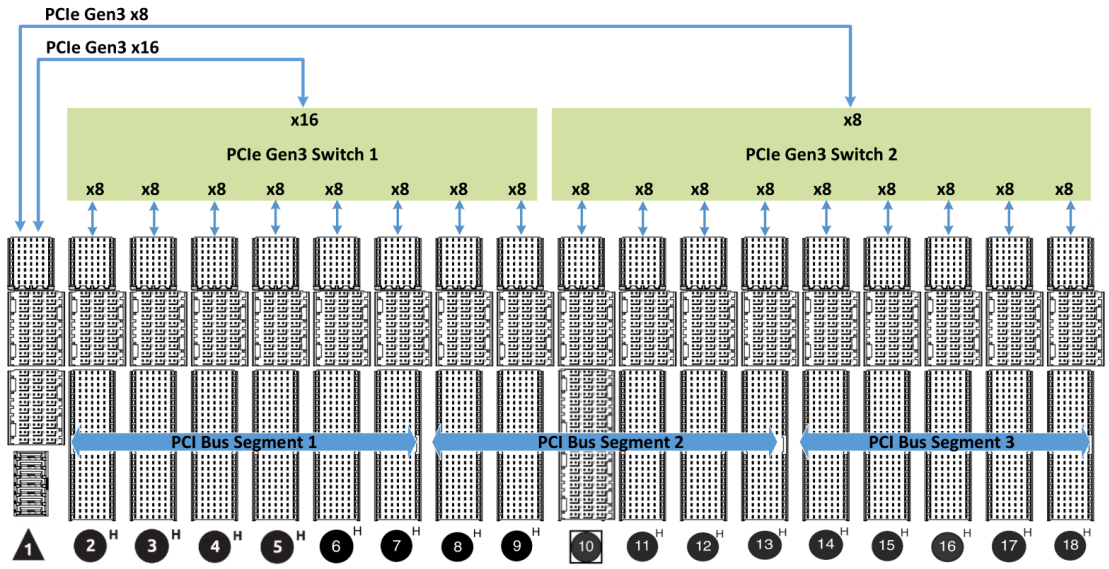

Figure 1 PXIe-2723 Gen3 Backplane Architecture

2.1.2 PXIe-2723G2 Backplane Architecture

The system slot can support PCIe Gen2 x16 link (x8 + x8), it has a maximum system bandwidth of 8 GB/s. Four of the PXIe peripheral slots have a PCIe Gen2 x8 link providing a maximum slot bandwidth of 4 GB/s. The 13 remaining peripheral slots have a PCIe Gen2 x4 link providing a maximum slot bandwidth of 2 GB/s.

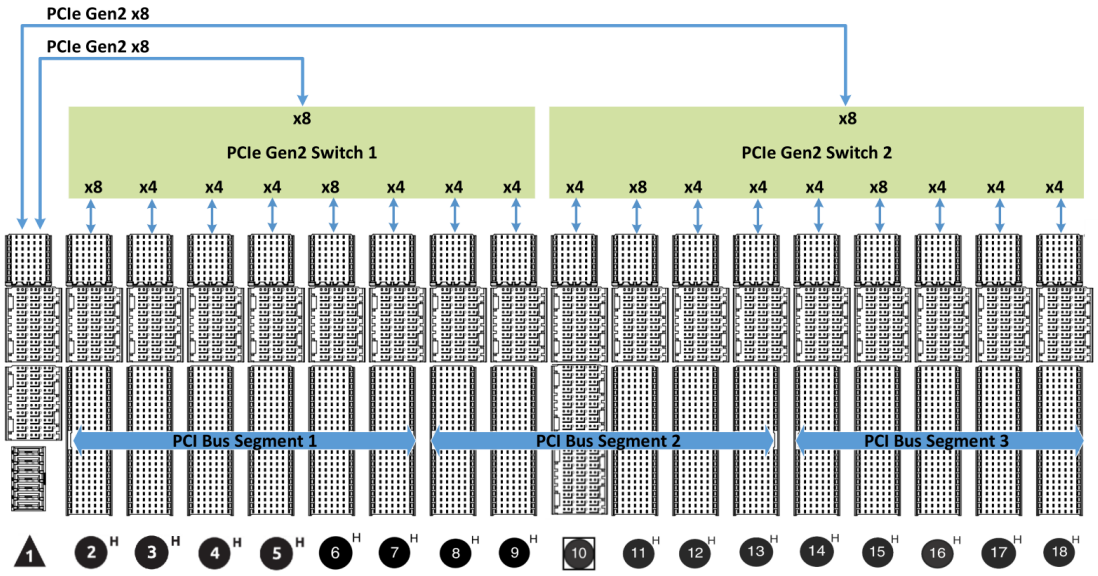

Figure 2 PXIe-2723 Gen2 Backplane Architecture

Note:

- Slot2, slot6, slot11 and slot15 can support PCIe Gen2 x8, the remaining peripheral slots can support PCIe Gen2 x4.

2.1.3 System Controller Slot

The System Controller slot is a fixed PCIe 2-Link configuration. Link 1 and Link 2 are routed to PCIe switch board, and then downstream to every peripheral slot. The chassis can accommodate a maximum 4-slot width PXIe controller.

2.1.4 System Timing Slot

The System Timing slot, designated as Slot 10, provides one dedicated single-ended star trigger and three pairs of differential star trigger lines to each peripheral slot. The routing for the single-ended star trigger signals (PXI_STAR) and differential star trigger signals (PXIe_DSTAR) is as follows.

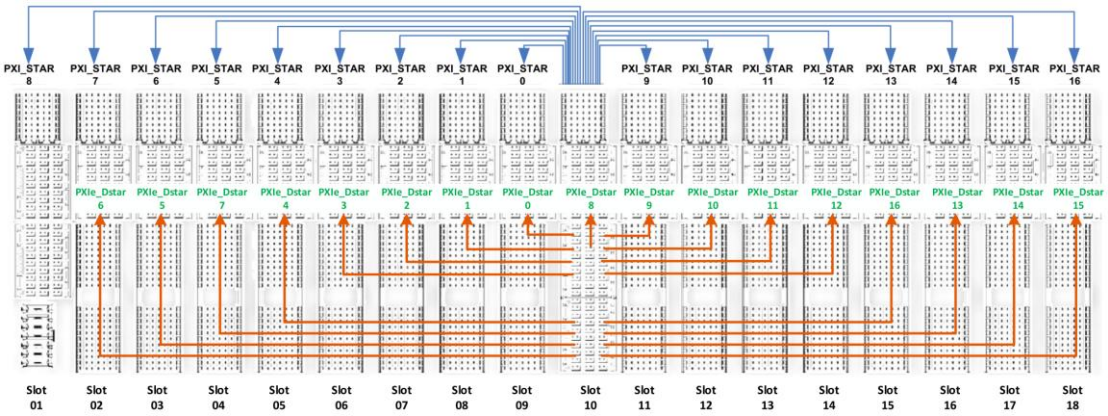

Figure 2 Star Trigger & Differential Star Bus Routing

Slot	PXI_Star	PXIe_DStar
1	8	N/A
2	7	6
3	6	5
4	5	7
5	4	4
6	3	3
7	2	2
8	1	1
9	0	0
10	N/A	8
11	9	9
12	10	10
13	11	11
14	12	12
15	13	16
16	14	13
17	15	14
18	16	15

Table 2 Star Trigger & Differential Star Bus Assignments

2.1.5 Peripheral Slot

PXIe-2723 provides seventeen hybrid peripheral slots. It can accept the following peripheral modules:

- PXI Express Peripheral Module
- CompactPCI Express Type-2 Peripheral Module
- Hybrid slot compatible PXI-1 Peripheral Module
- CompactPCI 32-bit Peripheral Module

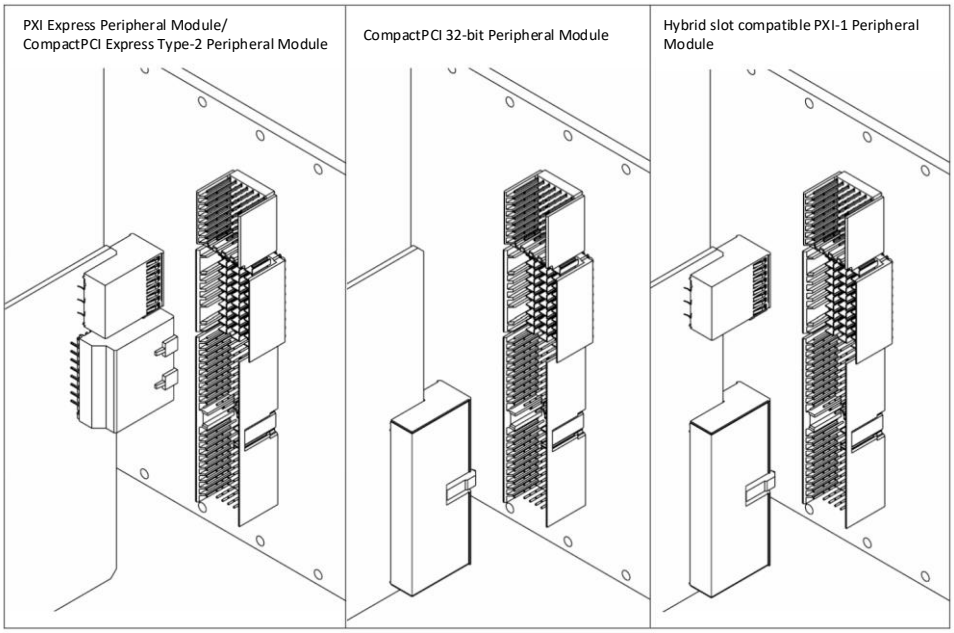

Figure 3 PXIe-2723 Peripheral Slot Compatible Modules

Each peripheral slot PCIe link can support Gen3 x8 (PXIe-2723G3) or Gen2 x8 (PXIe-2723G2), providing maximum single-direction bandwidth of 8GB/s or 4GB/s. And each peripheral slot can also support 32bit PCB bus, providing maximum single-direction bandwidth of 132MB/s.

2.1.6 PXI Trigger Bus

Three trigger bus segments on the PXIe-2723 consist of a first segment from 1st to 6th slots, a second from 7th to 12th slots, and a third from 13th to 18th slots, with each trigger bus segment containing 8 trigger lines connecting all slots on the same segment, providing inter-module synchronization.

Trigger bus buffers can connect or disconnect the trigger lines of adjacent segments. As shown in Figure 5, eight combinations of trigger bus segment connections are possible between the three bus segments, with any applicable to each of the eight trigger lines.

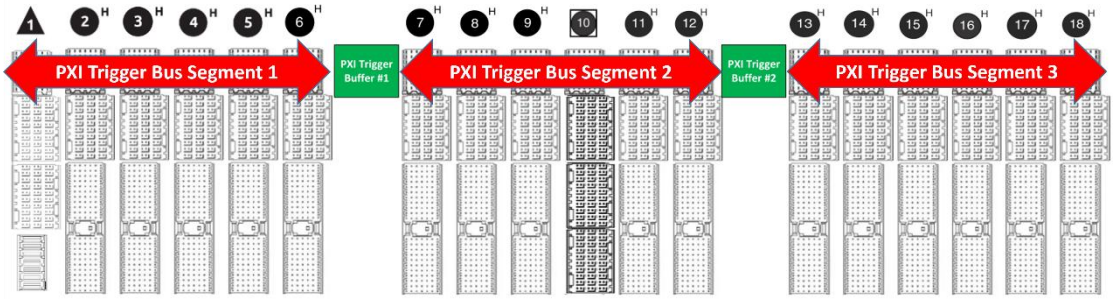

Figure 4 PXI Trigger Bus Connectivity Diagram

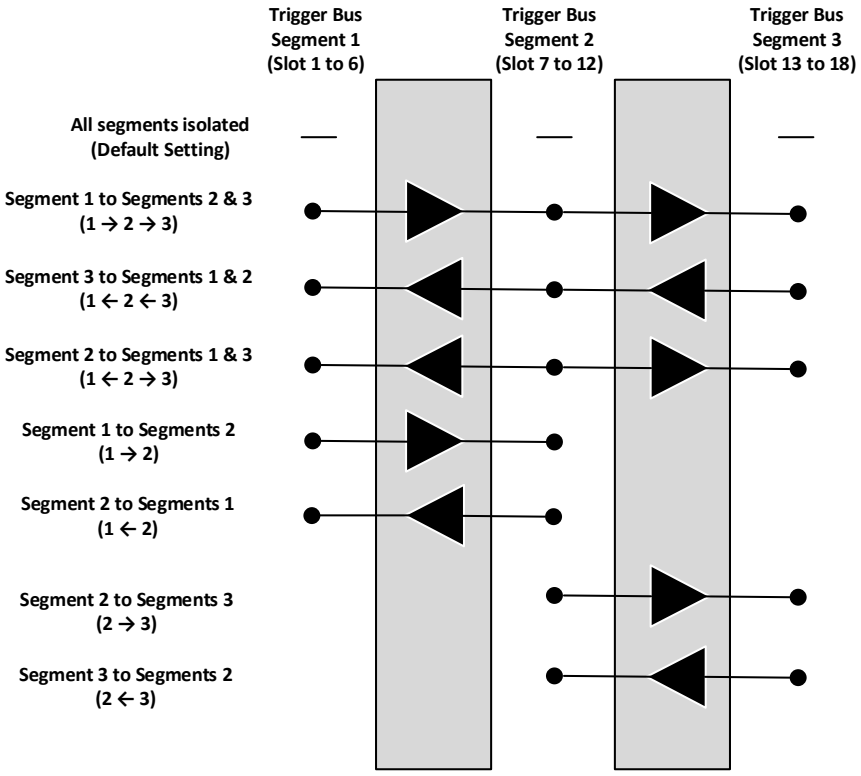

Figure 5 Trigger Bus Buffer Routing

Note:

- The triangle shown represents the direction of the trigger.
- The trigger bus buffer routing can be configured via the JYDM utility.

2.1.7 PXI Local Bus

The local bus on PXIe-2723 is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right, which by routing PXI Local Bus 6 signal between adjacent peripheral slots.

2.1.8 System Reference Clock and Synchronization Signal

The PXIe-2723 backplane supplies 10MHz reference clock (PXI_CLK10), 100MHz reference clock (PXIe_CLK100) and synchronization signal (PXIe_SYNC100) to each peripheral slot for inter-module synchronization.

The PXI_CLK10 and PXIe_CLK100 clocks are in-phase according to the PXI-5 specification. A phase-lock loop (PLL) circuit on the backplane synchronizes the PXI_CLK10 and PXIe_CLK100 clock.

The PXIe-2723 PXI chassis automatically selects the 10 MHz reference clock source from among:

- Built-in 10 MHz clock source on backplane.
- External 10 MHz clock through front panel's SMA connector.
- PXI_CLK10_IN pin on the system timing slot (slot 10)

Priorities for 10MHz reference clock are as follows.

System Timing Slot (10th slot)	SMA Connector on Front Panel	10MHz Clock Source of Peripheral Slots
No clock present	No clock present	Backplane's local oscillator
No clock present	10MHz clock present	SMA connector
10MHz clock present	No clock present	System timing slot
10MHz clock present	10MHz clock present	System timing slot

Table 2 Reference Clock Priority

The PXIe-2723 has the default timing relationship of PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 as show in Figure 4 which comply with PXI-5 specification.

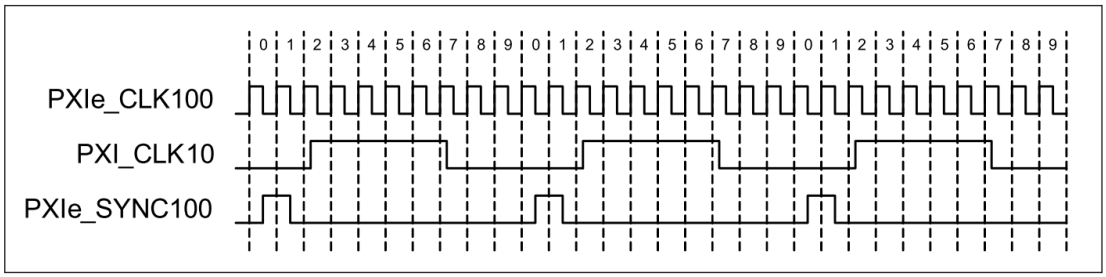

Figure 6 System Reference Clock Default Behavior

2.2 Specifications

2.2.1 Basic

Descriptions	PXIe-2723G3	PXIe-2723G2
PXI Chassis Type	PXIe	PXIe
Slot Count	18	18
Maximum slot bandwidth	8 GB/s (PCIe Gen3 x8)	4 GB/s (PCIe Gen2 x4 or x8)
Maximum system bandwidth	24 GB/s (PCIe Gen3 x24)	8 GB/s (PCIe Gen2 x16)
Chassis Power Supply Type	AC	AC
Slot Cooling Capacity	58 W (0°C ~ 40°C) 38W (0°C ~ 55°C)	58 W (0°C ~ 40°C) 38W (0°C ~ 55°C)
Onboard Clock Type	TCXO	TCXO
External Clocking	Yes	Yes
Number of hybrid slots	16	16
System timing slot	1	1

Table 3 Basic Specification

2.2.2 Electrical

AC Input		
Descriptions	PXIe-2723G3	PXIe-2723G2
Total Chassis Power	1300 W	1300 W
Input voltage range	100 to 240 VAC	100 to 240 VAC
Input frequency	50/60 Hz	50/60 Hz
Input current rating	12-6 A	12-6 A
Efficiency	91%	91%

DC Output		
Descriptions	PXIe-2723G3	PXIe-2723G2
Total Available Power	1170W (0°C ~ 45°C , 220VAC) 990W (45°C ~ 55°C , 220VAC)	1170W (0°C ~ 45°C , 220VAC) 990W (45°C ~ 55°C , 220VAC)
+3.3 V	77 A	77 A
+5 V	53 A	53 A
+12 V	72 A	72 A
–12 V	4 A	4 A
5 Vaux	4 A	4 A
+3.3V Load Regulation	5%	5%
+5V Load Regulation	5%	5%
+12V Load Regulation	5%	5%
-12V Load Regulation	5%	5%
5Vaux Load Regulation	5%	5%
+3.3V Maximum Ripple and Noise	39 mVpp	39 mVpp
+5V Maximum Ripple and Noise	19 mVpp	19 mVpp
+12V Maximum Ripple and Noise	15 mVpp	15 mVpp
-12V Maximum Ripple and Noise	4 mVpp	4 mVpp
5Vaux Maximum Ripple and Noise	4 mVpp	4 mVpp

Maximum power dissipation		
System Controller Slot	140W	140W
Hybrid Peripheral Slot	58W	58W

System Controller Slot Current Capacity		
+3.3 V	15 A	15 A
+5 V	15 A	15 A
+12 V	30 A	30 A
5 Vaux	3 A	3 A
Hybrid Peripheral Slot with PXI-5 Peripheral Slot Current Capacity		
+3.3 V	9 A	9 A
+12 V	6 A	6 A
5 Vaux	1 A	1 A
Hybrid Peripheral Slot with PXI-1 Peripheral Slot Current Capacity		
+3.3 V	6 A	6 A
+5 V	6 A	6 A
+12 V	1 A	1 A
–12 V	1 A	1 A
V (I/O)	11 A	11 A

Table 4 Electrical Specification

2.2.3 System Synchronization Clock

PXI_CLK10	Maximum slot-to-slot skew	160 ps
	Accuracy	±1 ppm max
	Maximum jitter	3.5 ps RMS phase-jitter (10 Hz–1 MHz range)
	Duty-factor	45%–55%
	Unloaded signal swing	3.3 V ±0.3 V
PXIe_CLK100	Maximum slot-to-slot skew	125 ps
	Accuracy	±1 ppm max
	Maximum jitter	1.7 ps RMS phase-jitter (12 kHz–20 MHz range)
	Duty-factor	45%–55%
	Absolute differential voltage	400–1000 mV
PXIe_SYNC100	Maximum slot-to-slot skew	125 ps
	Accuracy	±1 ppm max
	Maximum jitter	3.6 ps RMS phase-jitter (12 kHz–20 MHz range)
	Duty-factor	45%–55%
	Absolute differential voltage	400–1000 mV

External 10 MHz Reference Output (SMA connector)	Accuracy	±1 ppm max
	Maximum jitter	3.3 ps RMS phase-jitter (10 Hz–1 MHz range)
	Output amplitude	1 VPP ±20% square-wave into 50 Ω
		2 VPP unloaded
	Output impedance	50 Ω ±5 Ω
External 10 MHz Reference Input (SMA connector)	Frequency	10 MHz ±100 PPM
	Input amplitude	100 mVPP to 5 VPP square-wave or sine-wave
	Input impedance	50 Ω ±5 Ω

Table 5 System Synchronization Clock

2.2.4 Physical and Enviornment

Operating Environment		
Descriptions	PXIe-2723G3	PXIe-2723G2
Maximum altitude	3048 m	3048 m
Ambient temperature range	0 to 55 °C	0 to 55 °C
Relative humidity range	10 to 90%, noncondensing	10 to 90%, noncondensing

Storage Environment		
Descriptions	PXIe-2723G3	PXIe-2723G2
Ambient temperature range	-40˚C to 70˚C	-40 ˚C to 70 ˚C
Relative humidity range	5% to 95%	5% to 95%

Shock and Vibration	
Operational shock	30 g peak, half-sine, 11 ms pulse duration
Random Vibration (Operating)	5 to 500 Hz, 0.3 Grms, 3 axes
Random Vibration (Nonoperating)	5 to 500 Hz, 2.46 Grms, 3 axes

Sound Pressure Level		
Descriptions	PXIe-2723G3	PXIe-2723G2
Auto fan (up to ~25 °C ambient)	46 dBA	46 dBA
High fan	64 dBA	64 dBA

Sound Power		
Descriptions	PXIe-2723G3	PXIe-2723G2
Auto fan (up to ~25 °C ambient)	56 dBA	56 dBA
High fan	76 dBA	76 dBA

Backplane		
Descriptions	PXIe-2723G3	PXIe-2723G2
Size	3U	3 U

Chassis Size and Weight		
Descriptions	PXIe-2723G3	PXIe-2723G2
Width	440.2 mm	440.2 mm
Depth	455.2 mm	455.2 mm
Height	177.8 mm	177.8 mm
Net Weight	12.65 kg	12.65 kg
Gross Weight (with package, power cable)	16.55 kg	16.55 kg

Table 6 Physical and Environment

2.3 Mechanical Dimensions

All dimensions are shown in mm (millimeters)

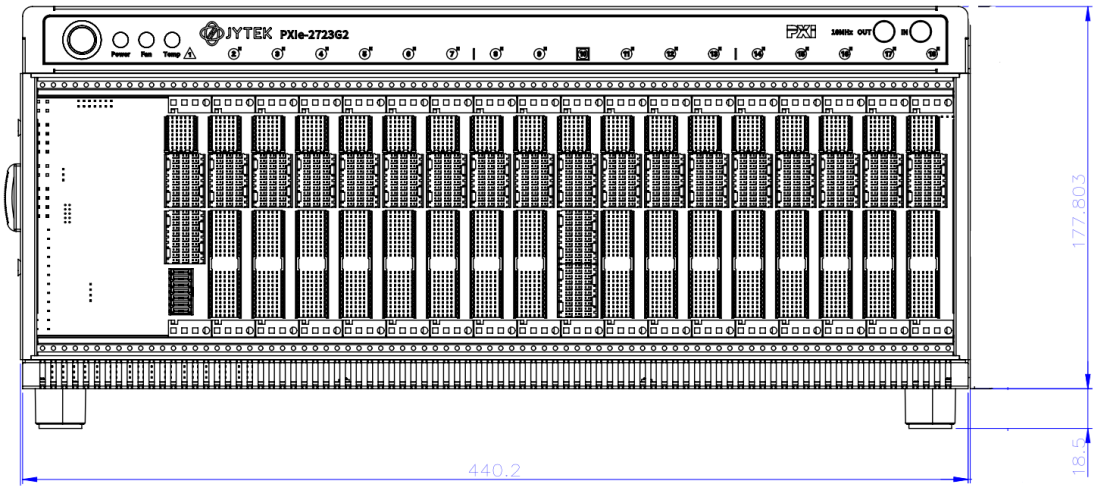

Figure 7 Front View

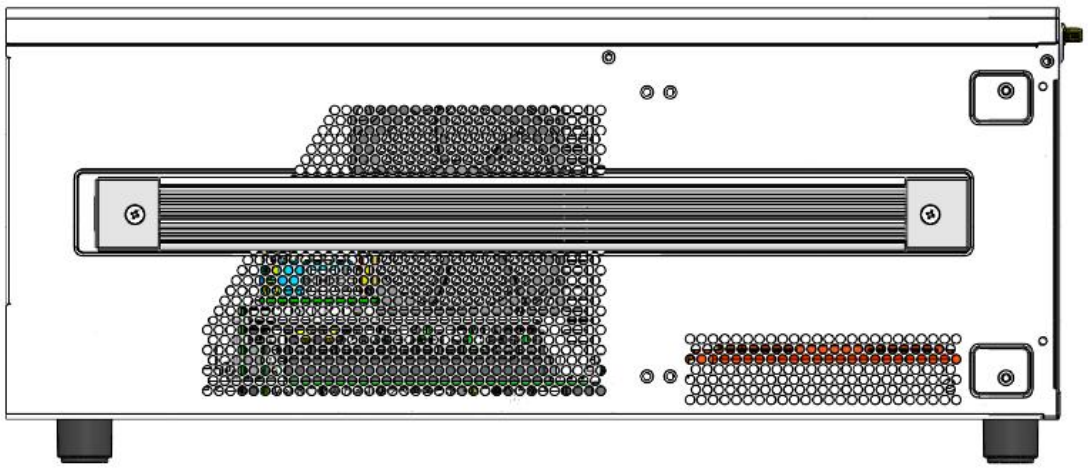

Figure 8 Left Side View

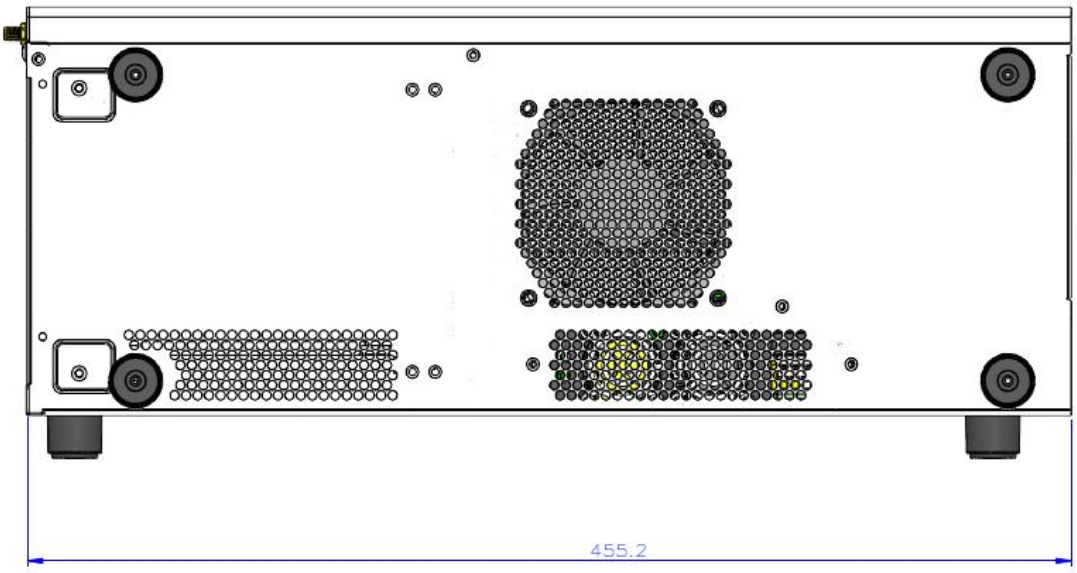

Figure 9 Right Side View

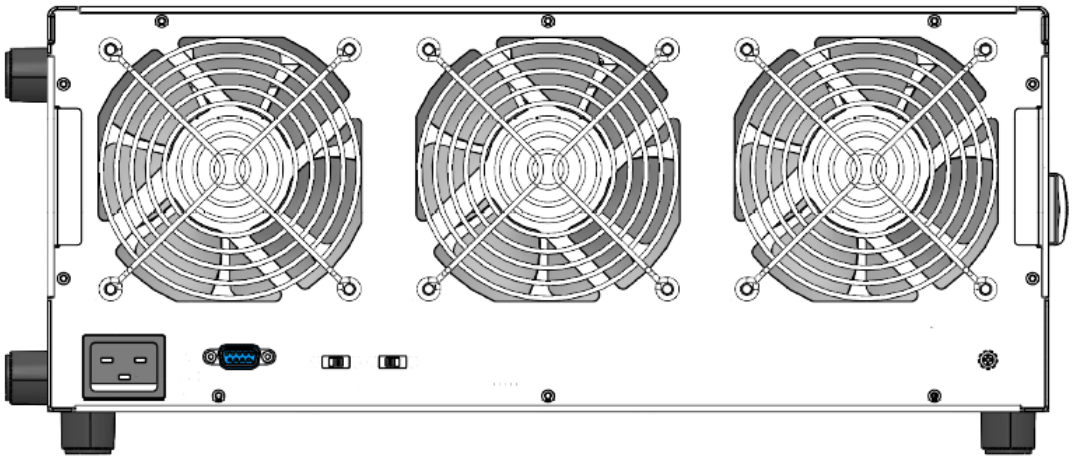

Figure 10 Rear View

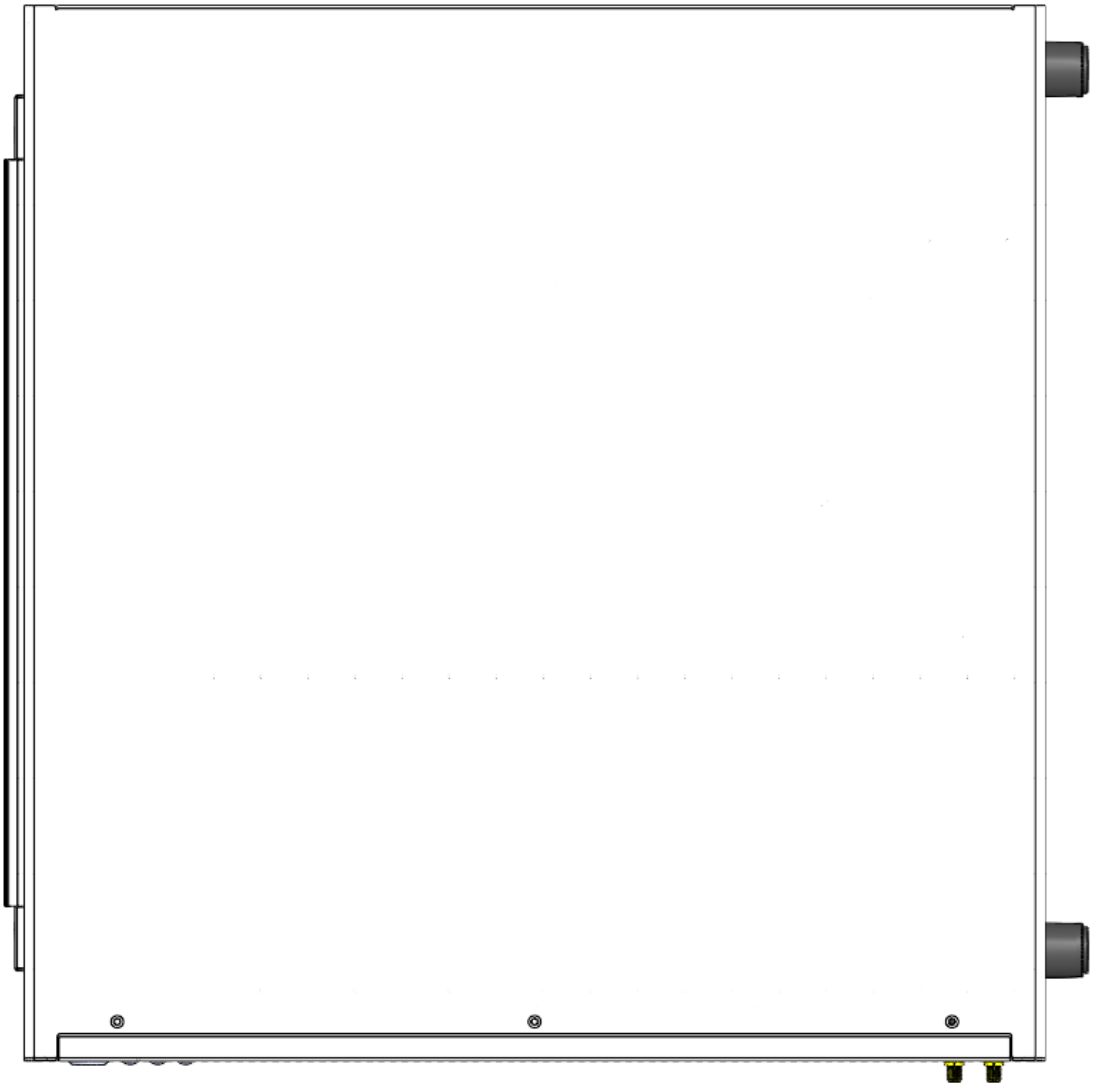

Figure 11 Top View

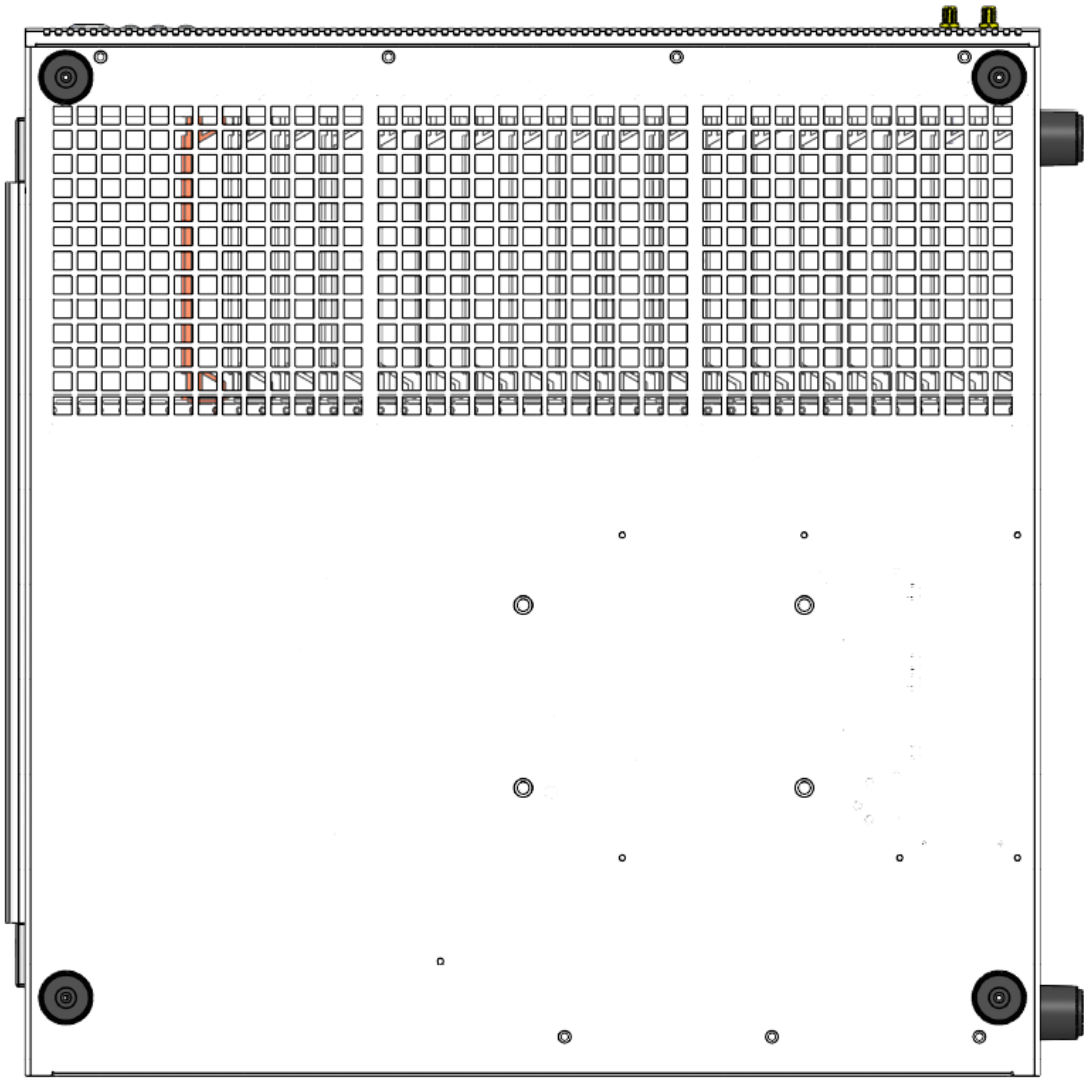

Figure 12 Bottom View

2.4 Front and Rear Panels

2.4.1 Front Panel

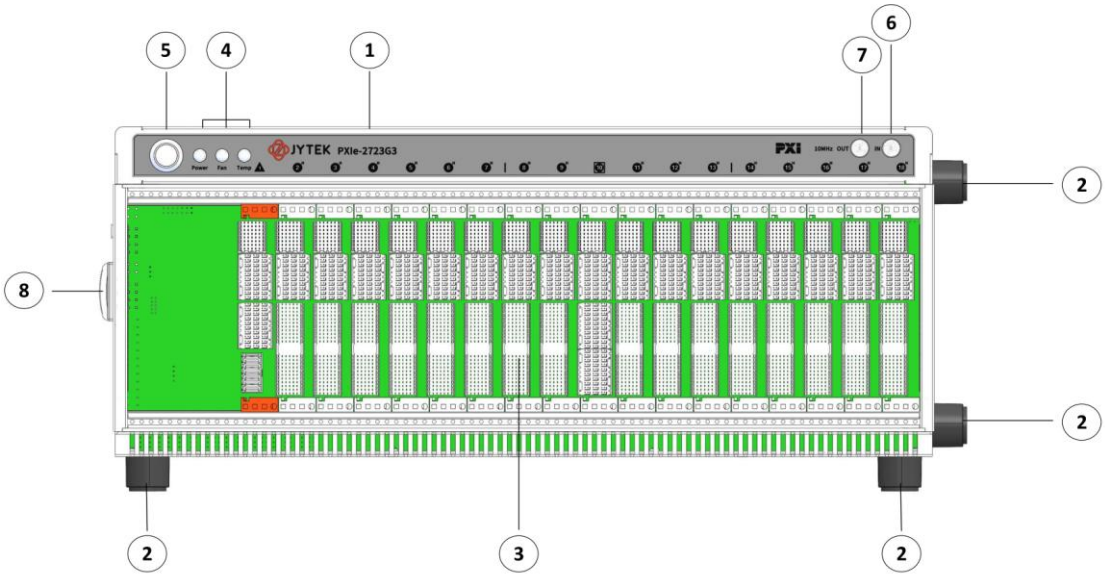

Figure 13 Front Panel

Location	Feature
1	Chassis Model Name
2	Removable Feet
3	Backplane Connectors
4	Chassis Status LED
5	Power Switch
6	10MHz REF CLK IN
7	10MHz REF CLK OUT
8	Handle

Table 7 Front Panel

2.4.2 Rear Panel

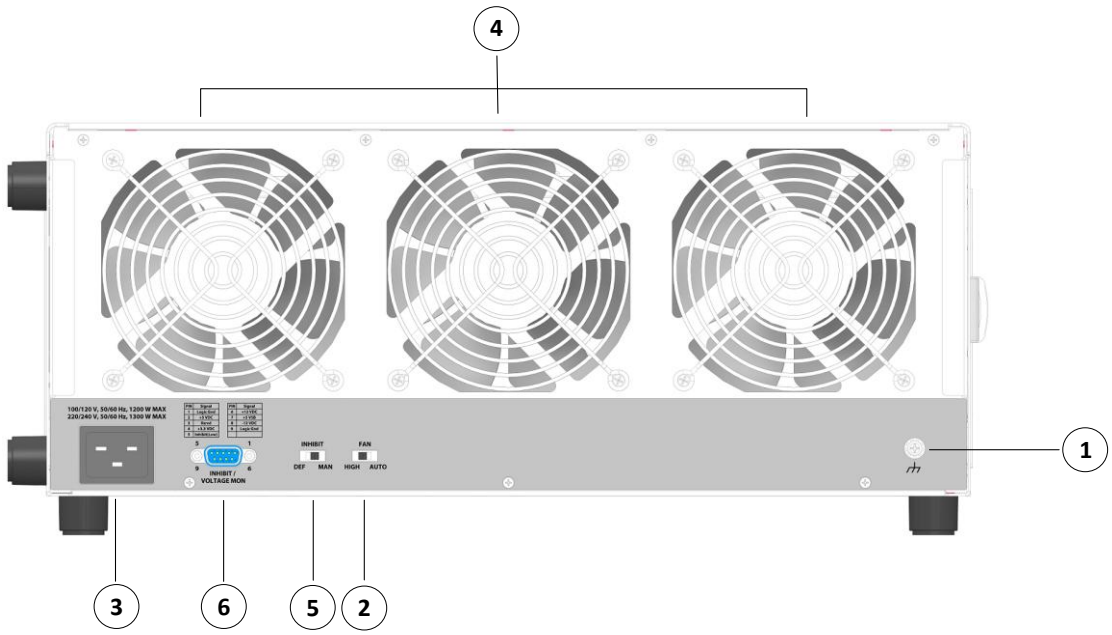

Figure 14 Rear Panel

Location	Feature
1	Chassis Ground Screw
2	FAN Switch
3	AC Input
4	Rear Output Vents
5	Inhibit Switch
6	Inhibit/Voltage Monitoring DB-9 Connector

Table 8 Rear Panel

2.4.3 Inhibit/Voltage Monitoring DB-9 Connector

The DB-9 connector monitors the four main power rails via digital multimeter. Power rail pin assignments shown in Figure 15. There are 10 kΩ current-limiting resistors on each power rail prevents accidental overload. One Inhibit (active low) pin is provided to power the chassis on/off when the Inhibit Switch is in the MAN (manual) position, such that chassis is powered on when Inhibit pin is logic high or open, and off when Inhibit pin is grounded.

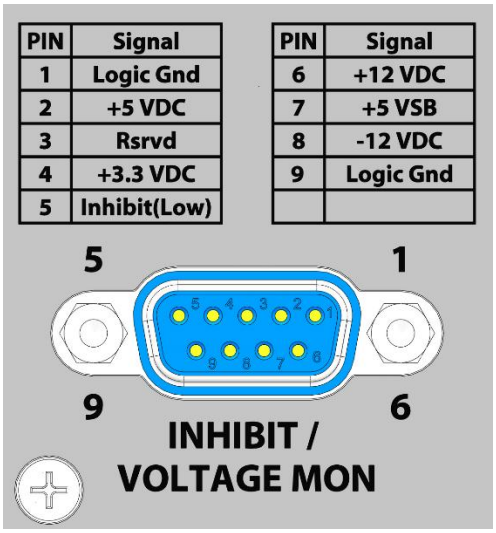

Figure 15 Inhibit/Voltage Monitoring DB-9 Connector

2.4.4 Inhibit Switch

In the **DEF** (default) position, the front panel power button turns the power supply on/off, and in the **MAN** (manual) position, the **Inhibit** pin on the DB-9 connector turns the power supply on/off.

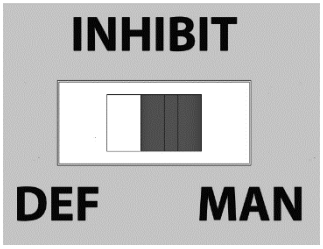

Figure 16 Inhibit Switch

2.4.5 FAN Switch

In the **HIGH** position, fans operate at maximum speed, and in **AUTO,** the fans run based on the monitored chassis temperature.

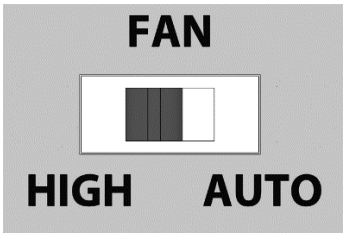

Figure 17 FAN Switch

2.4.6 Chassis Status LED

Chassis Status LED	Temp LED (Amber)	Fan LED (Green)	Power LED (Blue)
On	Chassis MCU is abnormal	Fan is normal	Power is normal
Off	Temperature is normal	Chassis is powered down	Chassis is powered down
Blinking	Temperature sensors exceeds threshold temperature (default is 70℃)	Fan falls below threshold speed (default is 800RPM)	Power rail exceeds threshold setting (default is ±5%)

Table 9 Chassis Status LED

2.4.7 Fan Mode

PXIe-2723 provides the smart fan control mechanism as blow curve. It provides two fan modes.

Fan Mode	Fan's duty cycle	Fan's speed	Note
AUTO	40% ~ 100%	1680 rpm ±10% to 4200 rpm ±10%	Based on temperature sensors.
HIGH	100%	4200 rpm ±10%	

Table 10 Fan Mode

When the **Fan Switch** is set to **AUTO** mode, the fan speed is controlled based on the measured temperature of sensor.

Fans run at 40% duty cycle if the measured temperature less than 25°C, and begin ramping up when any temperature reading exceeds 25°C.

Fans run at 100% duty cycle (full speed) if any temperature reading exceeds 50°C.

When the **Fan Switch** is set to **HIGH** mode, fans run at 100% duty cycle immdiately.

The factory default fan control curve shows as following Figure.

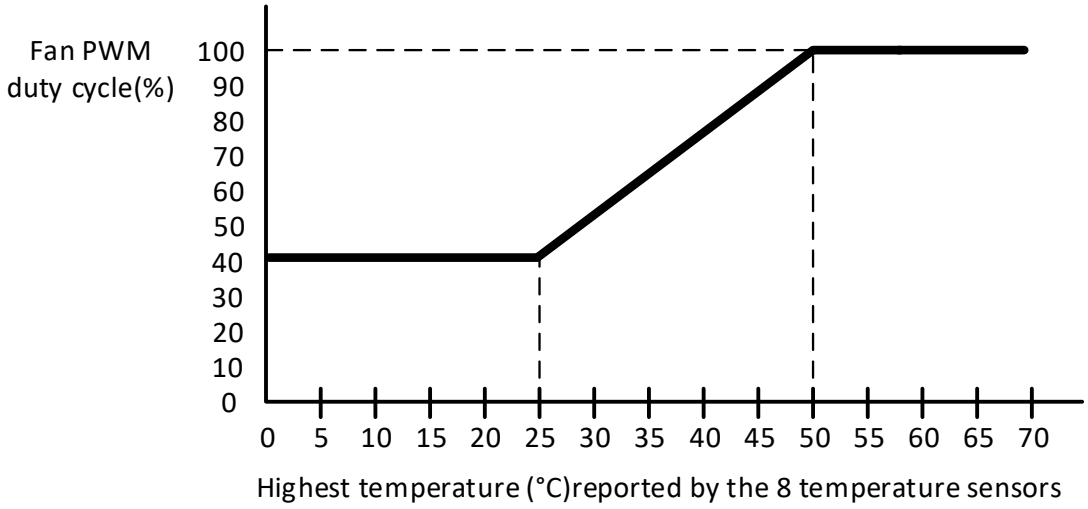

Figure 18 Fan Control Curve

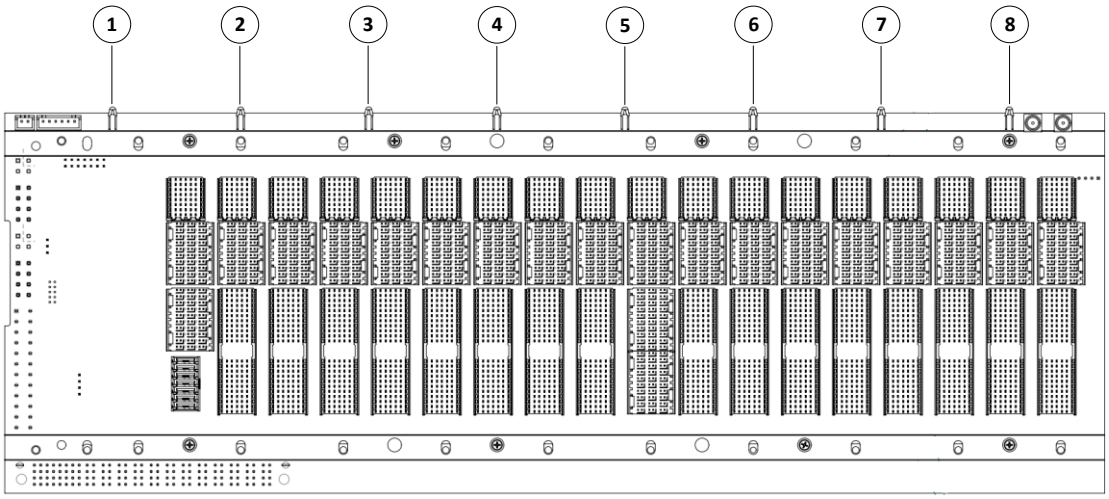

Figure 19 Position of temperature sensors

Note:

- For details about chassis temperature monitoring, please see JYDM utility on page 32.

2.5 Chassis Cooling Considerations

2.5.1 PXI/PXIe Modules Cooling

For PXI/PXIe modules cooling, there are three fans on the rear panel draw cool air from the bottom side and front panel to be exhausted to the rear panel.

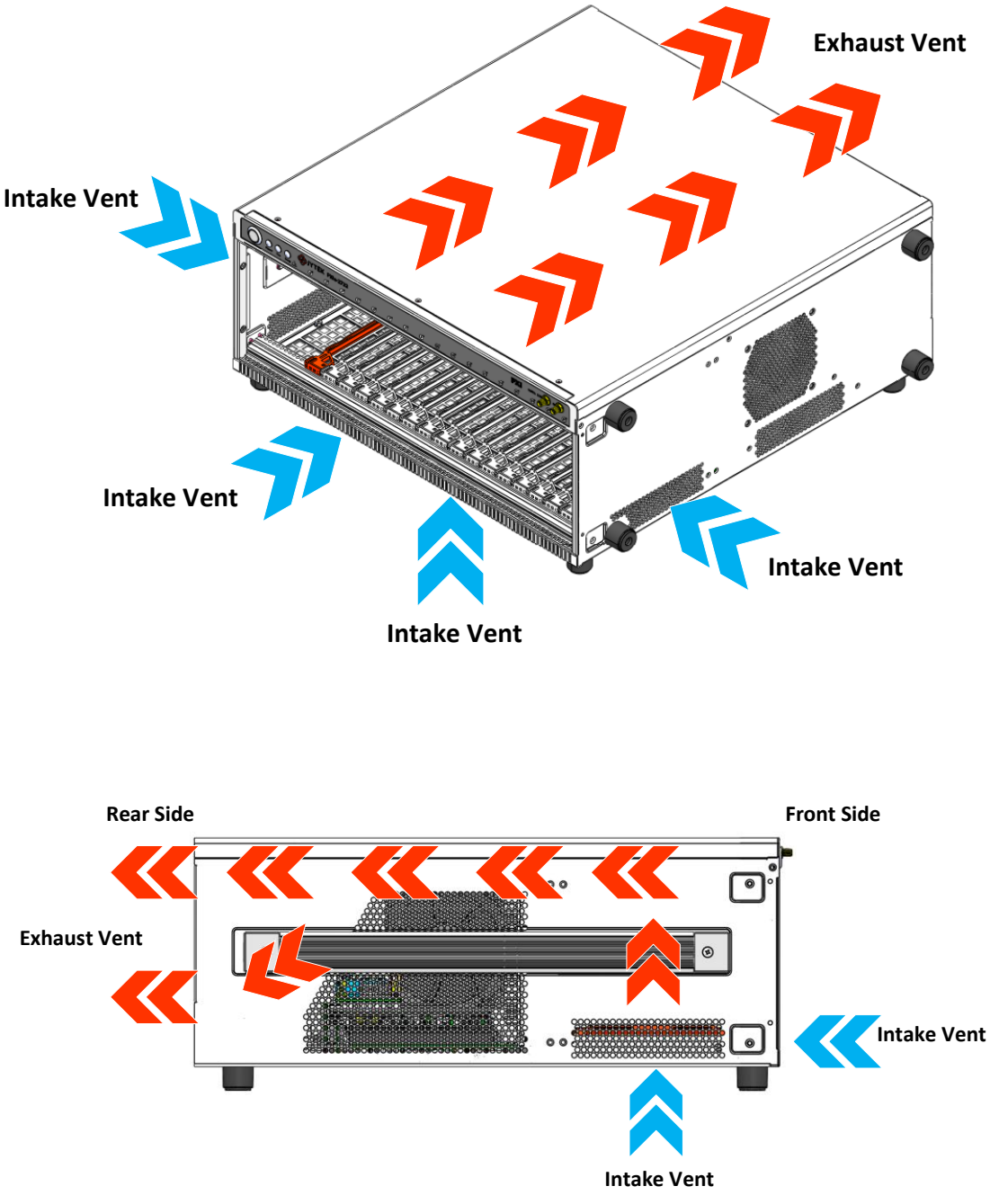

Figure 20 PXI/PXIe Modules Cooling

2.5.2 Power Supply Cooling

For power supply cooling, power supply's fan draws cool air from the right side, to be exhausted through the left side of the chassis.

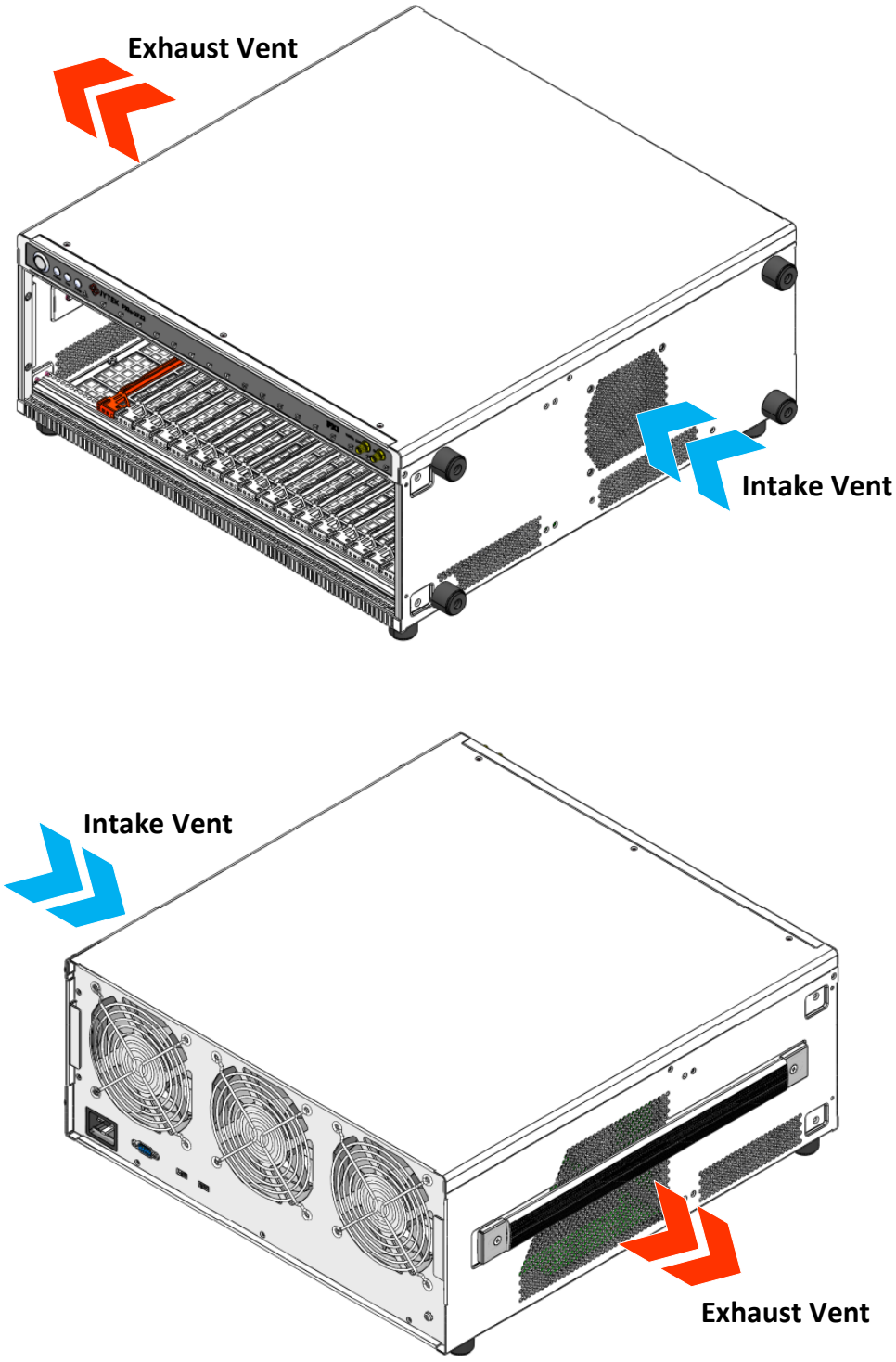

Figure 21 Power Supply Cooling

3. Software

3.1 Introduction to JYDM

JYDM (**JY**TEK **D**evice **M**anagement) is the latest equipment management software of JYTEK. Its main functions are as follows:

- Support GUI information display and management of PXI-2/6 standard equipment.
- Support trigger configuration of PXI-9 standard chassis.
- JYTEK self-developed chassis information management.
- JYTEK self-developed card: alias management, driver and firmware online upgrade, online driver version management, board test panel.
- JYTEK SeeSharp card: driver information view, test panel.

3.2 Installation and use of JYDM

JYDM support operating system: Windows 7 32/64 bit, Windows 10 32/64 bit.

1. Install **.Net framework** (version 4.0 or above).
2. Download and install **FirmDrive** (version 1.3.3 or above) from the official website of JYTEK.
3. Download and Install the JYTEK **peripheral module driver** from the official website of JYTEK.
4. Download and install the **JYDM** installation package from the official website of JYTEK.

Figure 22 Install the JYDM

After the software installation complete, open JYDM and you will see the chassis, controller and peripheral module in the overall system as shown in the figure below.

Note:

- JYDM usually requires a few seconds to scan device.

The left side of the JYDM interface is the hardware device column, and the right side is the device details column. You can view and configure the current device information, and upgrade the driver and firmware.

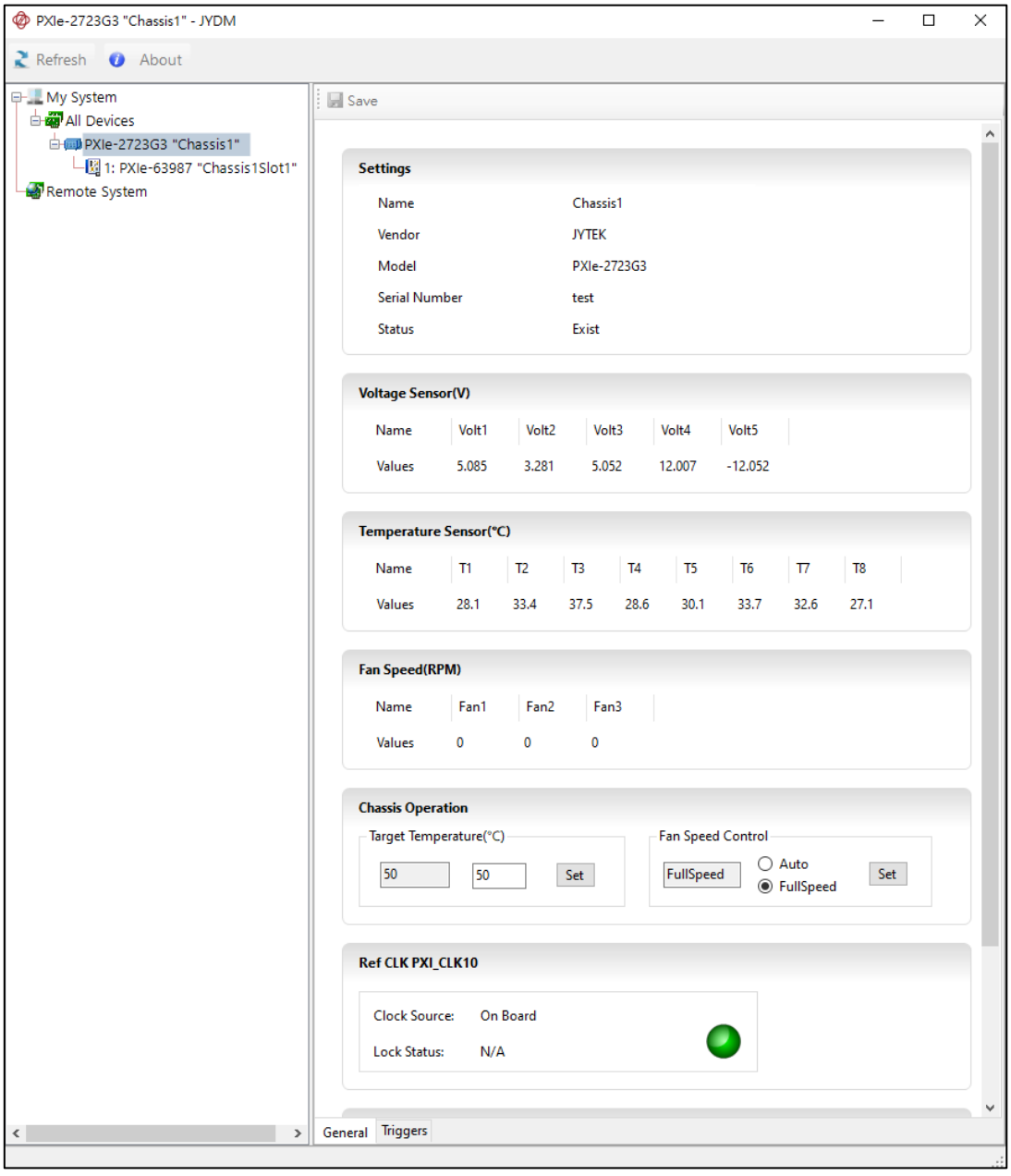

Figure 23 JYDM GUI application program

Note:

- JYTEK peripheral module driver has two parts: the shared common driver kernel software (FirmDrive) and the specific peripheral module driver.
- After firmware update of peripheral module, you need to **cold restart** your device.
- After driver update of peripheral module, you need to **warm restart** your device.

3.3 Chassis environment monitoring in JYDM

The JYDM provides the following chassis environment monitoring capabilities:

- Monitoring the chassis power rails: 5Vsb (standby power), 3.3V, 5V, 12V and -12V DC power.

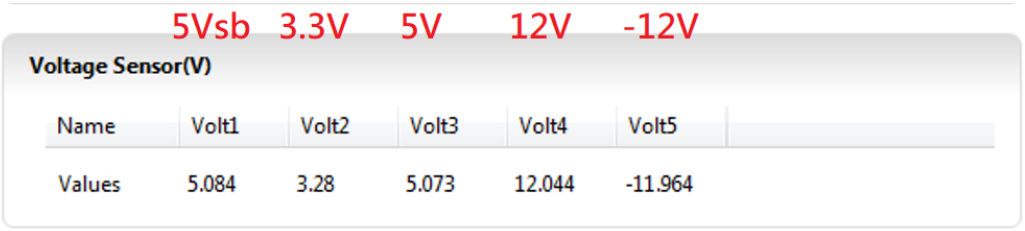

Figure 24 Monitoring the Chassis Power Rails

- Monitoring the chassis temperature sensors.

  (T1 sensor is located on the top side of backplane, close to slot1.)

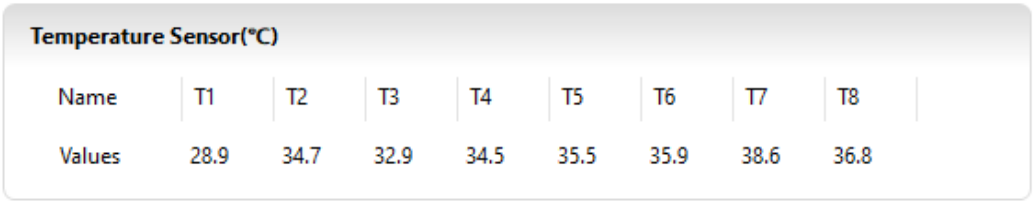

Figure 25 Monitoring the Chassis Temperature Sensors

- Monitoring the chassis fan speed.

  (Fan1 module ia located on the rear side of chassis, close to slot1.)

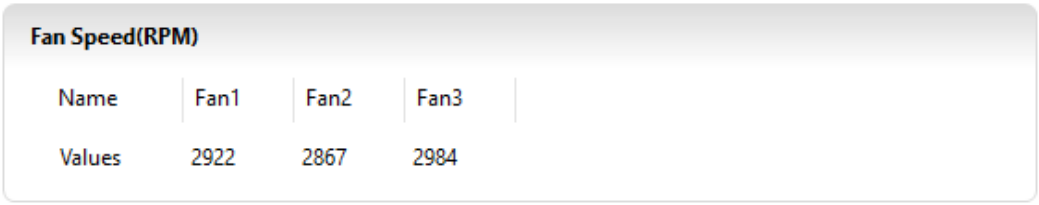

Figure 26 Monitoring the Chassis Fan Speed

3.4 Chassis cooling control in JYDM

PXIe-2723 chassis allow user to control the cooling capability via JYDM.

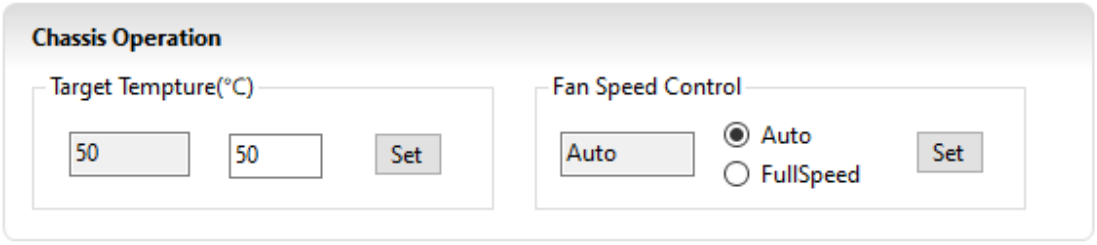

Figure 27 Chassis Cooling Control in JYDM

Target Temperature specifies the chassis temperature at which the maximum fan speed (100% duty cycle) is achieved as shown in below figure.

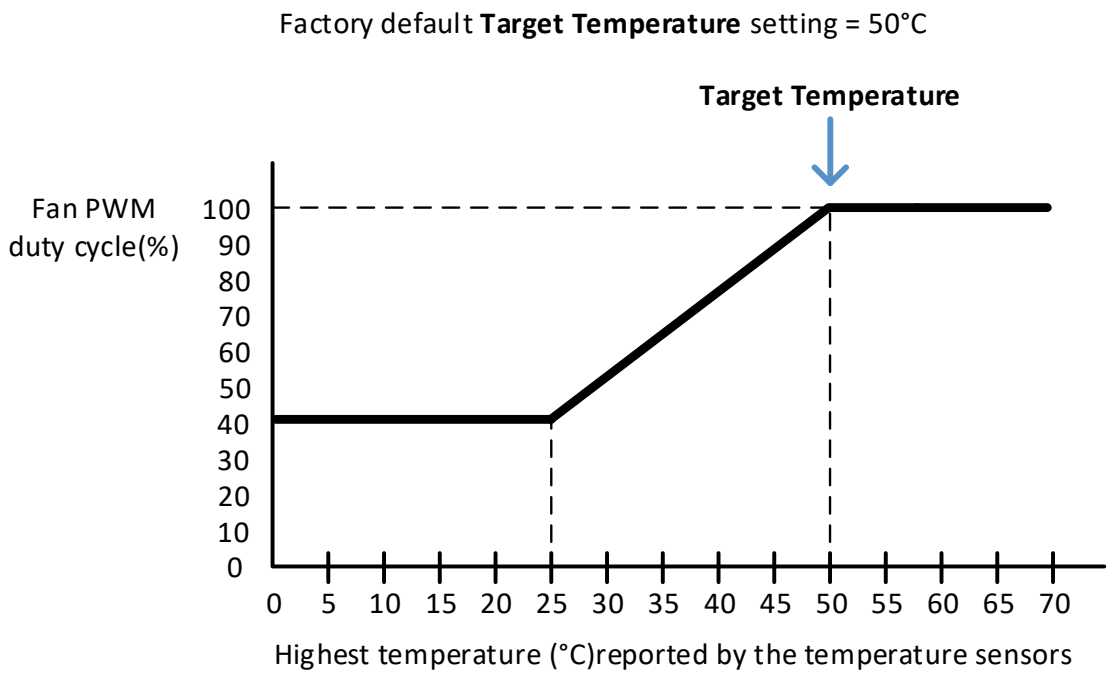

Figure 28 Factory default Target Temperature setting

The factory default target temperature setting is 50°C. User can change target temperature to lower value (ex. 40°C), it will increase fan speed if the factory default setting could not fulfill the peripheral modules cooling requirement.

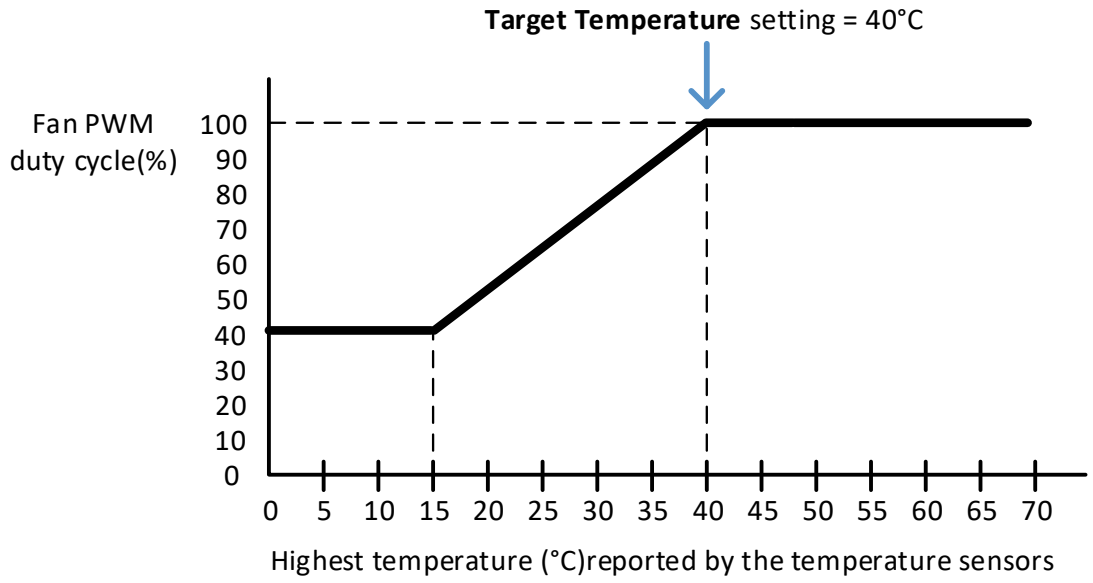

Figure 29 Change Target Temperature to 40°C

3.5 Reference Clock Status Display in JYDM

JYDM can display the 10MHz reference clock(PXI_CLK10) source which come from onboard (backplane's local oscillator) or external (front panel's SMA connector). The default clock source is **On Board** as shown in figure 33.

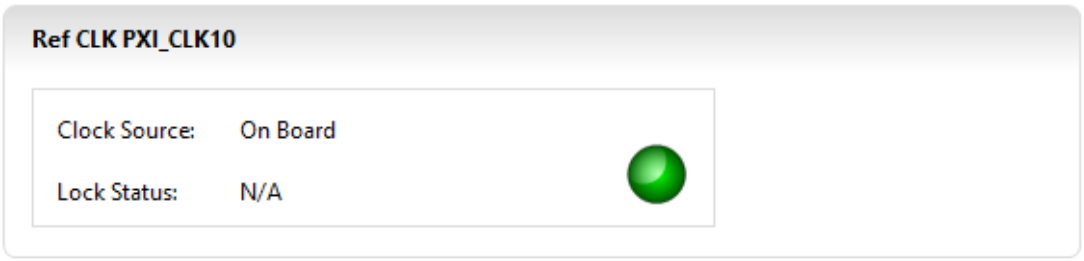

Figure 30 Reference Clock Status Display for default setting

If the external 10MHz clock input the chassis via SMA conncector, or 10MHz clock from system timing slot, it will override the onboard 10MHz clock. A phase-lock loop (PLL) circuit on the backplane synchronizes the PXIe_CLK100 and external 10MHz clock, and then JYDM will display **Synchronized** and green indicator as shown in figure 34.

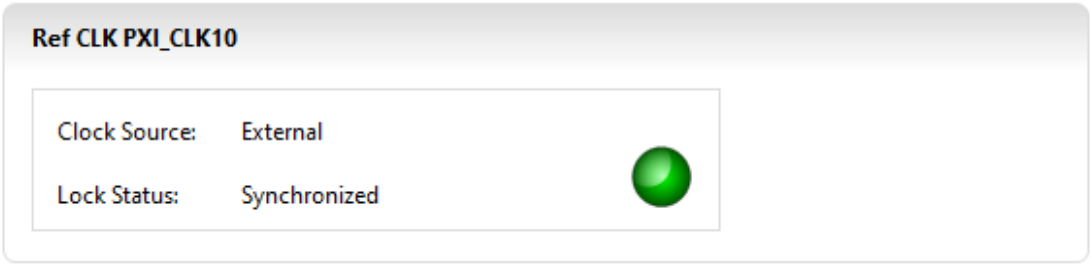

Figure 31 Reference Clock Status Display for external clock source

3.6 Trigger Bus Routing Control in JYDM

PXIe-2723 provides an interface to route PXI trigger bus. User can complete the following steps to route these trigger lines in JYDM.

1. Clicking on **My System** item, set **Default PXI Trigger Manger** to **JYTEK**, and then click **Save** to save the settings.
2. Clicking on the PXI chassis branch, and then click on the **Triggers** tab.
3. Select which trigger lines you would like to change routing.
4. Clicking on **Save** button.

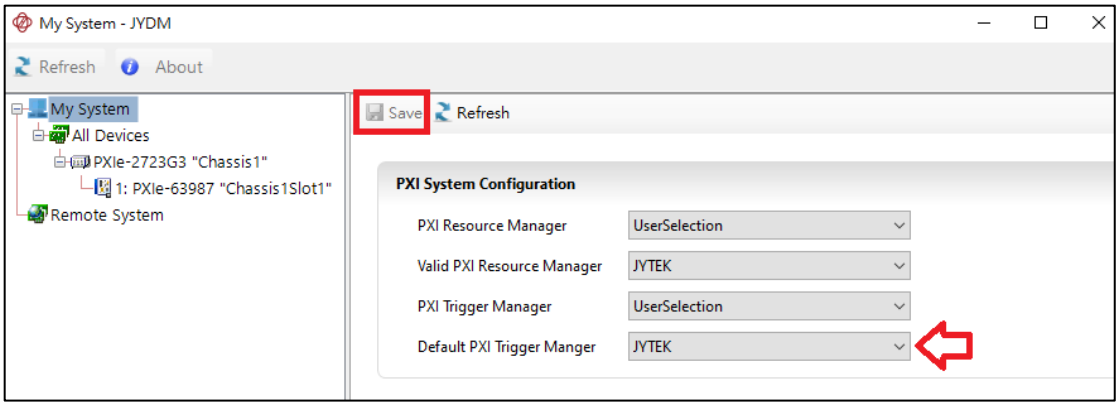

Figure 32 Change PXI Trigger Manager Setting To JYTEK

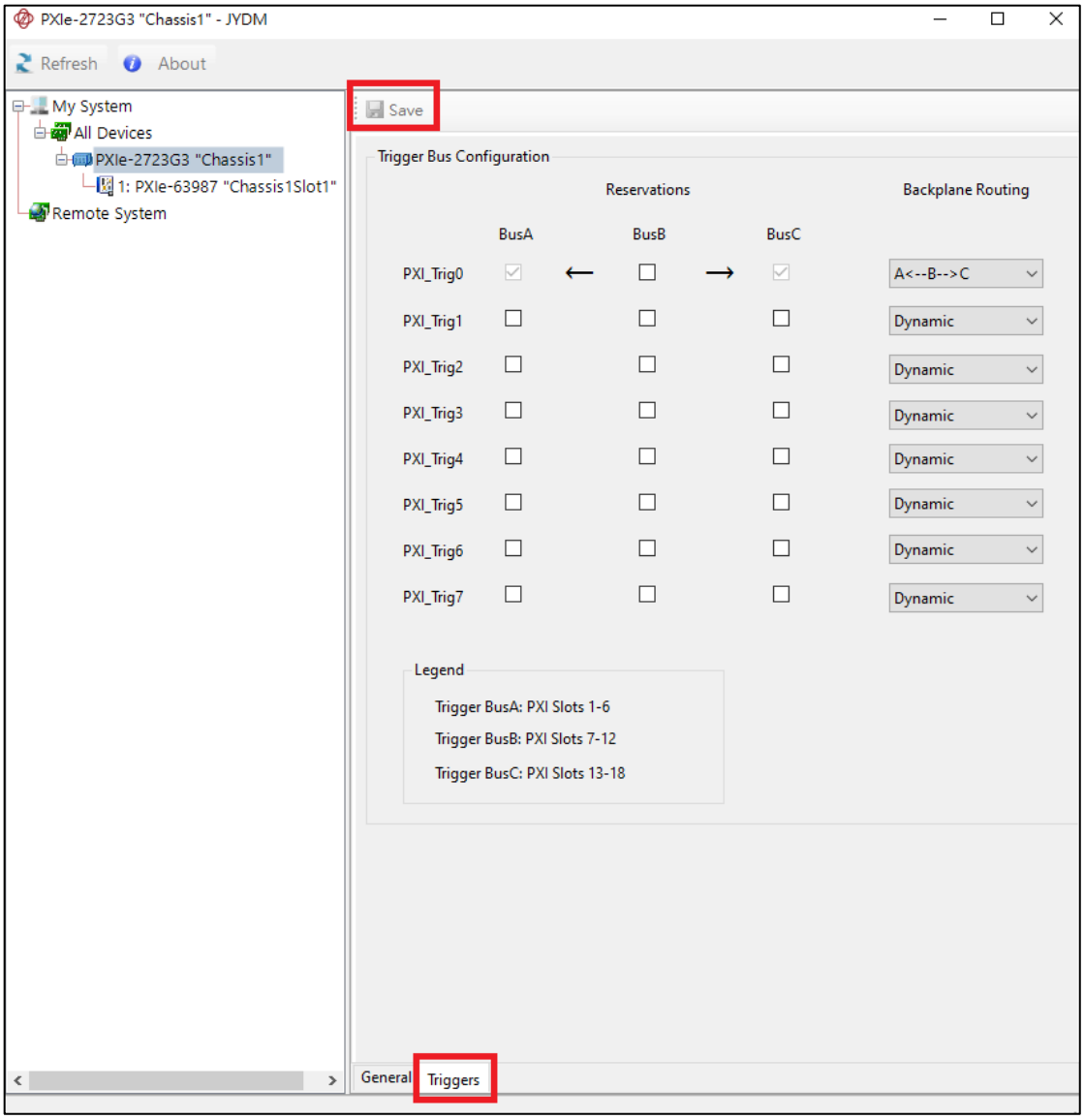

Figure 33 Trigger Bus Routing Control

3.7 Chassis identification in NI MAX

Download and install NI PXI platform services 20.0 or higher from NI website:

Figure 34 Install NI MAX

Open **JYDM**, set **Valid PXI Resource Manager** and **Default PXI Trigger Manger** to National Instruments, and then click **Save** to save the settings.

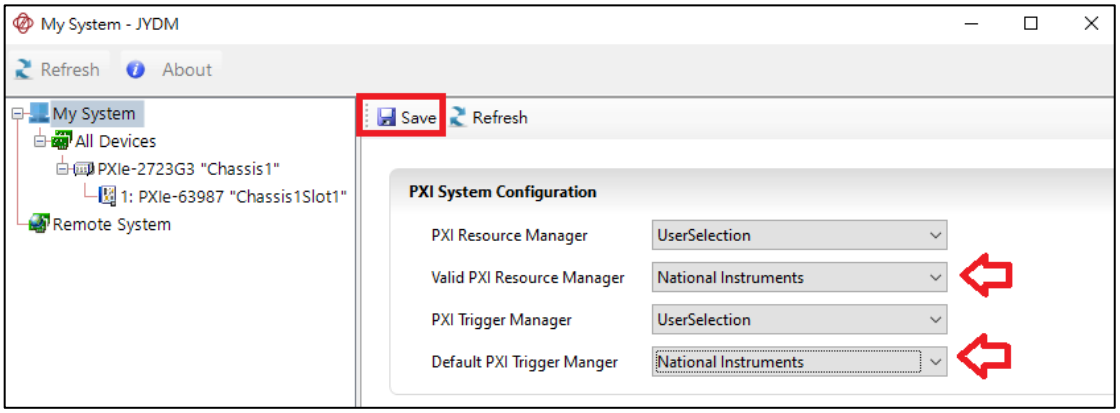

Figure 35 Change PXI Trigger Manager Setting

Open NI MAX after software installation and the devices can be identified:

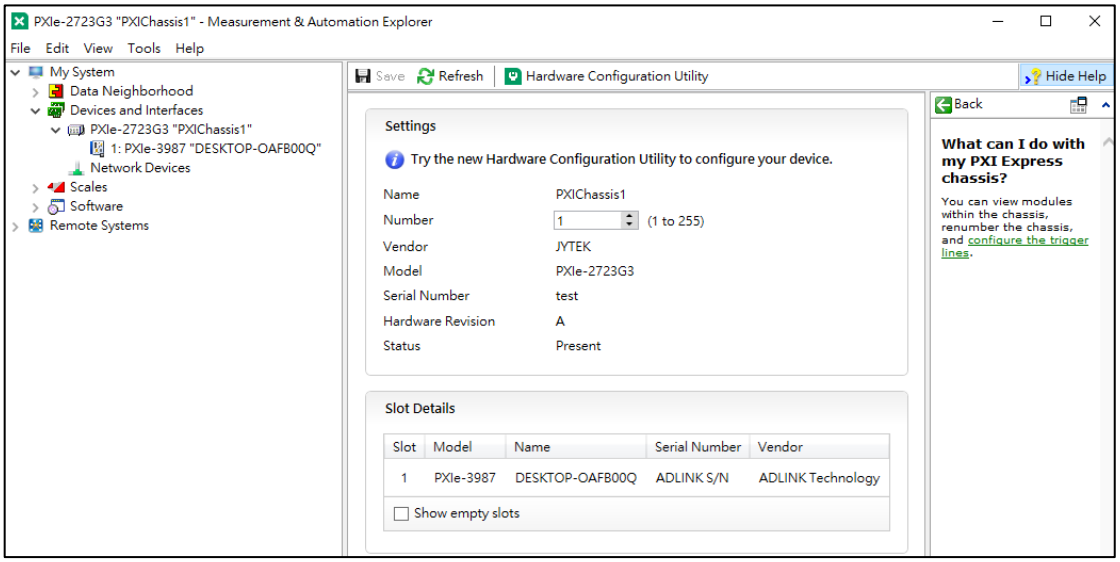

Figure 36 NI MAX GUI display JYTEK chassis and modules

4. Using PXIe-2723 Chassis

This chapter provides the operation guides for PXIe-2723.

4.1 Using PXIe-2723 with JYTEK PXI/PXIe Peripheral Modules

Using PXIe-2723 with JYTEK PXI/PXIe peripheral modules is straightforward. JYTEK also provide a device management software to view the modules in the chassis. For more information, please visit our web www.jytek.com to download.

4.2 Using PXIe-2723 with National Instruments PXI/PXIe Peripheral Modules

4.2.1 Use National Instruments PXI/PXIe Peripheral Modules without synchronization:

You can use the modules as usual without any additional setting. Chassis may not display correctly in NI MAX, but this will afftect nothing with module functions.

4.2.2 Use National Instruments PXI/PXIe Peripheral Modules with synchronization:

A few vi like" Get Full Terminal Name.vi" cannot use on the third party chassis:

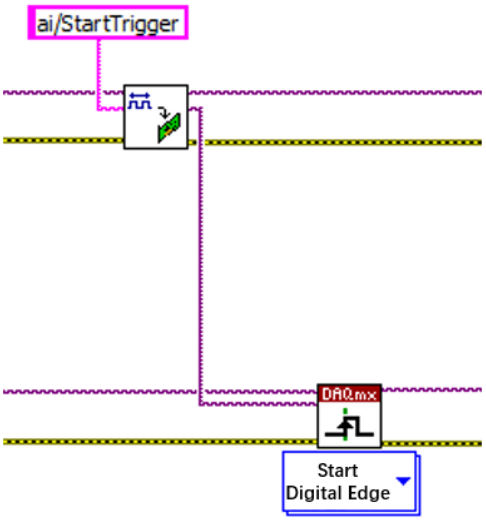

Figure 37 Trigger Routing

But you can use “DAQmx Export Signal” to set appointed clock/trigger routing:

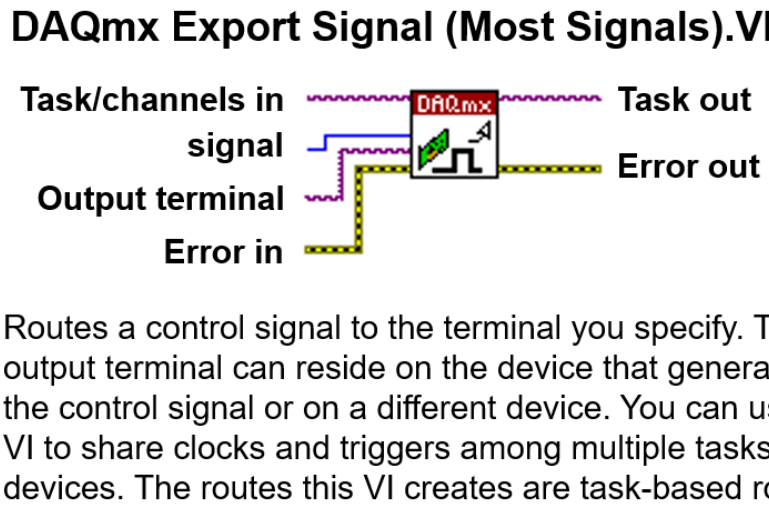

Figure 38 DAQmx Export Signal

DAQ synchronization reference code:

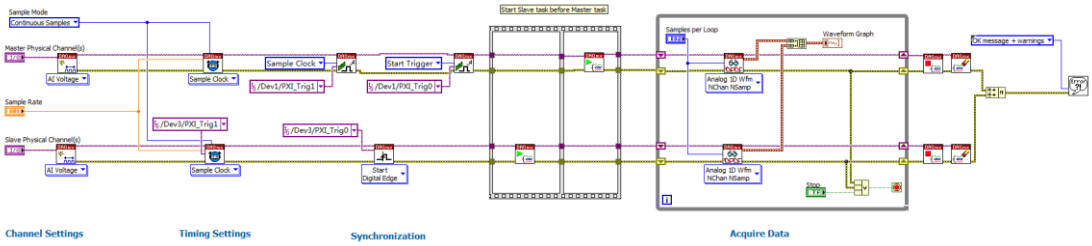

Figure 39 DAQ Synchronization Reference Code

5. Optional Equipment

5.1 Rack Mount Kits

JYTEK provides optional hardware for installation of PXIe-2723 chassis into a server or rack. The rack mounting kits dimension as following figure. All dimensions are shown in mm (millimeters).

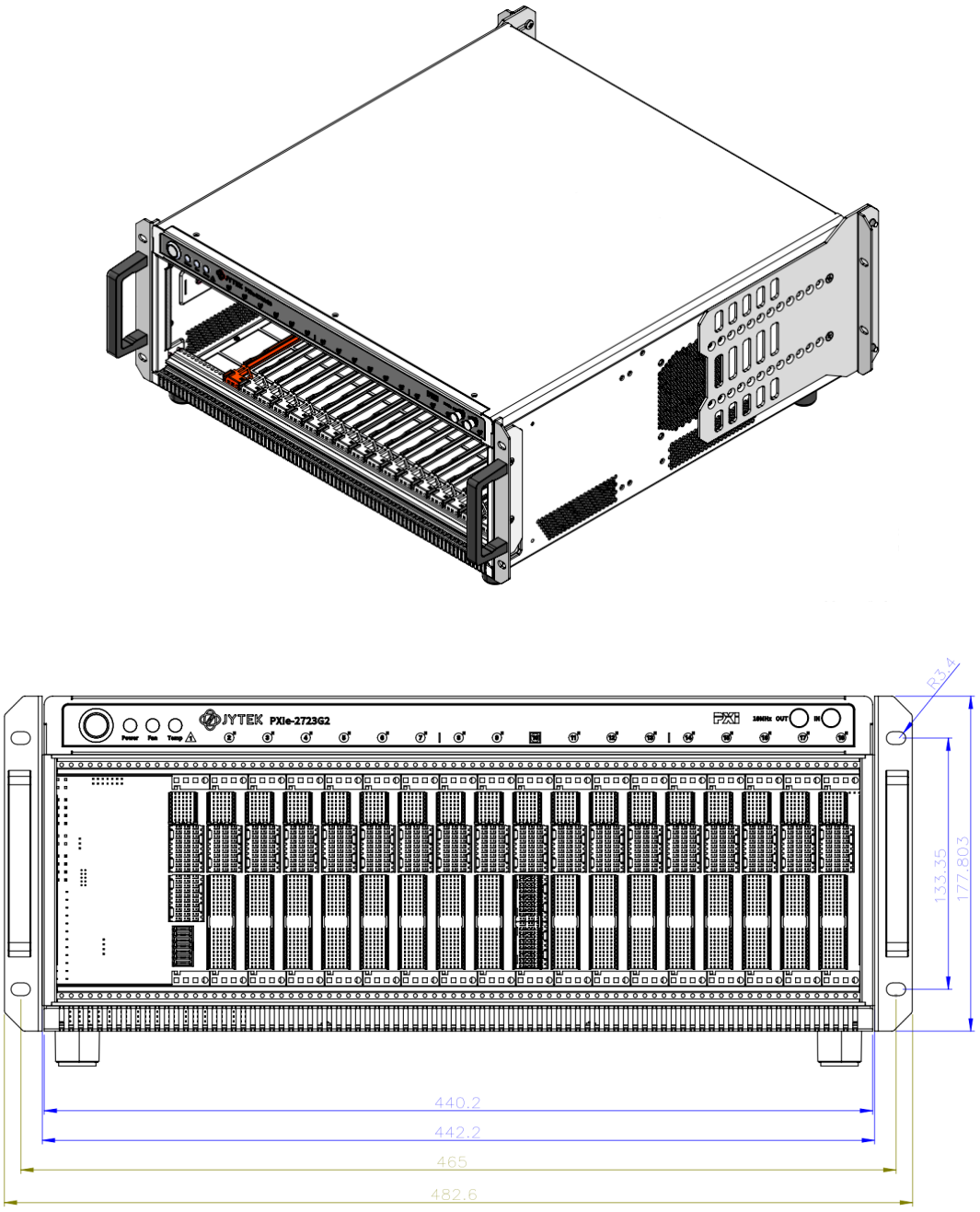

Figure 40 PXIe-2723 rack mount kits dimension

6. About JYTEK

6.1 JYTEK China

Founded in June, 2016, JYTEK China is a leading Chinese test & measurement company, providing complete software and hardware products for the test and measurement industry. The company is a joint venture between Adlink Technologies and a group of experienced professionals form the industry. JYTEK independenly develop the software and hardware products and is entirely focused on the Chinese market. Our Shanghai headquarters and production service center have regular stocks to ensure timely supply; we have R&D centers in Xi'an and Chongqing to develop new products; we also have highly trained direct technical sales representatives in Shanghai, Beijing, Tianjin, Xi'an, Chengdu, Nanjing, Wuhan, Haerbin, and Changchun. We also have many patners who provide system level support in various cities.

6.2 JYTEK Korea and JYTEK In Other Countries

JYTEK Korea was the first JYTEK enterprise outside China to promote JYTEK products. Together with Adlink Technologies and JYTEK China, JYTEK is expanding to more countries. Each JYTEK location is an independently owned and operated franchise. It shares JYTEK’s philosophy and business approach. Together JYTEK entities promote the JYTEK brand, technology, and products.

6.3 JYTEK Hardware Products

According to JYTEK’s agreement with our equity partner Adlink Technologies, JYTEK’s hardware is manufactured by the state-of-art manufacturing facility located in Shanghai Zhangjiang Hi-Tech Park. Adlink has over 20 years of the world-class low-volumn and high-mix manufacturing expertise with ISO9001-2008, China 3C, UL, ROHS, TL9000, ISO-14001, ISO-13485 certifications. Its 30,000 square meters facilities and three high-speed Panasonic SMT production lines can produce 60,000 pieces boards/month; it also has full supply chain management - planning, sweeping, purchasing, warehousing and distribution. Adlink’s manufacturing excellence ensures JYTEK’s hardware has word-class manufacturing quality.

One core technical advantage is JYTEK's pursue for the basic and fundamental technology excellence. JYTEK China has developed a unique PCIe, PXIe, USB hardware driver architecture, FirmDrive, upon which many our future hardware will be based.

In addition to our own developed hardware, JYTEK also rebrands Adlink's PXI product lines. In addition, JYTEK has other rebranding agreements to increase our hardware coverage. It is our goal to provide the complete product coverage in PXI and PCI modular instrumentation and data acquisition.

6.4 JYTEK Software Platform

JYTEK has developed a complete software platform, SeeSharp Platform, for the test and measurement applications. We leverage the open sources communities to provide the software tools. Our platform software is also open sourced and is free, thus lowering the cost of tests for our customers. We are the only domestic vendor to offer complete commercial software and hardware tools.

6.5 JYTEK Warranty and Support Services

With our complete software and hardware products, JYTEK is able to provide technical and sales services to wide range of applications and customers. In most cases, our products are backed by a 2-year warranty. For technical consultation, pre-sale and after-sales support, please contact JYTEK of your country.

7. Statement

The hardware and software products described in this manual are provided by JYTEK China, or JYTEK in short.

This manual provides the product review, quick start, some explaination for JYTEK PXIe-2723 chassis. The manual is copyrighted by JYTEK.

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While we try to keep this manual up to date, there are factors beyond our control that may affect the accuracy of the manual. Please check the latest manual and product information from our website.

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